QuikVoice™

Voice IC Chips Summary

QuikVoice IC chips are made with advanced CMOS LSI technology. They can record and/or play sounds stored in external memory chips including SRAM and EPROM. Sounds such as human voice, music and special sound effects can be faithfully captured and reproduced. Since these sounds are digitized, not synthesized, they sound as natural as the original.

CVSD Voice Compression

QuikVoice IC chips employs the Continuously Variable Slope Delta (CVSD) compression with sampling rates up to 128 Kbps. Frequency response up to 5 KHz may be achieved by using the highest sampling rate.

Minimum External Circuitry

QuikVoice IC chips require just a single 5V DC power supply to operate. External memory is accessed by the chips automatically, eliminating the need for a separate micro-controller. However, since these chips are designed to work with a wide range of sampling rates and output requirements, they don't have internal filters and power amplifiers. Therefore, external filter and power amplifier must be added to match the target sampling rate, frequency response and output requirement.

Unlimited Memory Expansion

All QuikVoice IC chips can access external memory of virtually unlimited amount. Which means a lot of messages or a very long message can be stored. Memory expansion is sometimes as easy as adding a binary counter chip in the design.

Multiple Message Support

The VP1410A, the VP1606 and the VP1608 all allow multiple messages of variable length to be stored in EPROM chips for random playback. Messages can be stored back to back in one or several EPROM chips, maximizing memory usage. The VP1000A is usually used for single-message applications only.

Dual Channel Audio Output

The VP1608 provides two channels of simultaneous audio output. These two outputs are available on separate pins and can be used independently or mixed together to form a single output. However, the dual output is not intended for stereo applications since the VP880 Voice Development System does not allow for stereo digitization.

Voice Developement System

For EPROM-based designs, either the VP880 Voice Development System or the VW1000A Voice EPROM Writer may be used for message digitization, editing and segment management. The resulted voice file is then downloaded into a standard EPROM programmer for EPROM programming. Eletech also provide voice digitization and EPROM programming service at low rates.

For SRAM based designs, the voice development tools are not needed because the recording circuitry is usually built into the design.

QuikVoice IC Chips Selection Guide

Model Number	Operation Mode	Max. # of Messages	No. of Channel	Supply Voltage	Memory Interface	Special Features
VP1000A	play/record	1	1	5 VDC	EPROM, SRAM	general purpose record and play
VP1410A	play	10	1	5 VDC	EPROM	individual trigger input pins
VP1606	play	64	1	5 VDC	EPROM	binary encoded trigger pins
VP1608	play	128	2	5 VDC	EPROM	binary encoded trigger, dual channel

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Quik VOICE

VP-1000A
Digital Voice Processor

FEATURES

- High quality voice & sound generation
- Record & playback with external SRAM
- Playback-only with external EPROM or ROM
- Stand-alone operation
- 32K x 8 direct memory addressing, expandable
- Single 5V DC supply voltage
- Low power consumption
- Continuous Variable Slope Delta (CVSD) modulation
- Sampling rate from 24Kbps to 128 Kbps
- Message digitization with the VP-880 or the VW-1000A
- Pin to pin compatible with UM5100
- 40-pin DIP (VP-1000A) or 48-pin QFP (VP-1000AF)

GENERAL DESCRIPTIONS

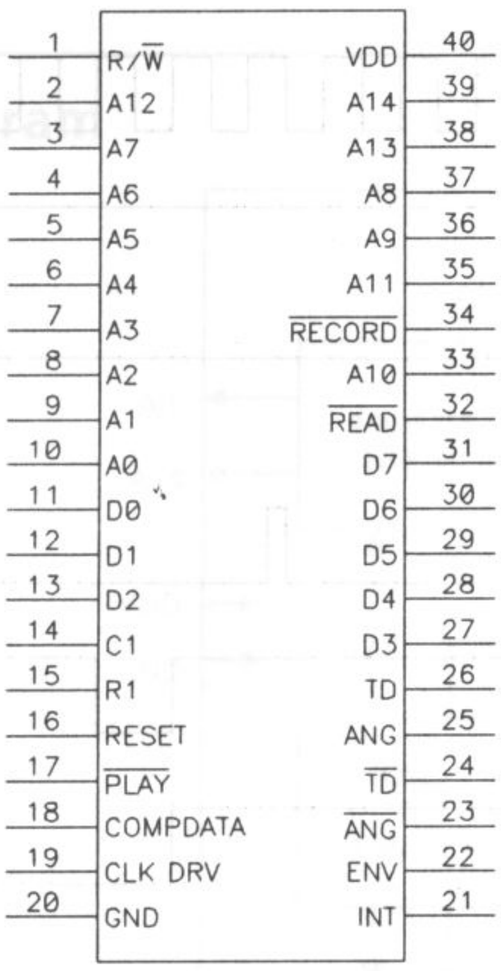
The VP-1000A is an advanced CMOS LSI chip for general purpose voice/sound record and playback applications. It can be interfaced with external SRAM to construct a realtime recording circuitry, or with external ROM or EPROM for playback only applications. When ROM or EPROM is used, the sound must be digitized by using Eletech's VP-880 Voice Development System or VW-1000A Voice EPROM Writer.

The VP-1000A is totally self-contained. It can access the external memory all by itself without the help from any microprocessor. Although the chip provides only 15 address lines, an external counter can be easily added to extend the memory addressing to virtuely no limitation. Therefore very long message length can be achieved easily. Overall, the VP-1000A offers high voice quality and flexible memory addressing that no other chips can.

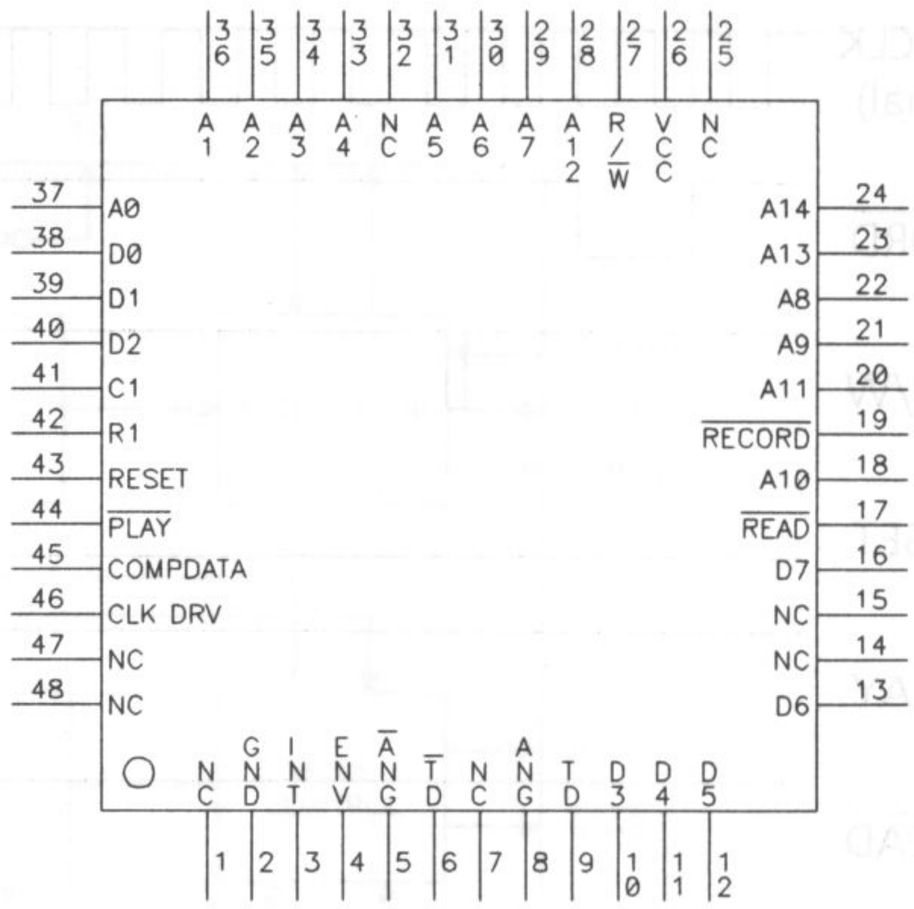
APPLICATIONS

- Voice memo recorder
- Sound effects generator
- Digital announcer for consumer, industrial, security and telecommunication products

VP-1000A (DIP40) Pin Assignment



VP-1000AF (QFP48) Pin Assignment



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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, V_{DD} - V_{SS} ..... 0 to 5.5V
Input Volotage, V_{IN} ..... V_{SS} to V_{DD}
Operating Temperature, T_{OP} ..... -10°C to 60°C
Storage Temperature, T_{ST} ..... -20°C to 80°C

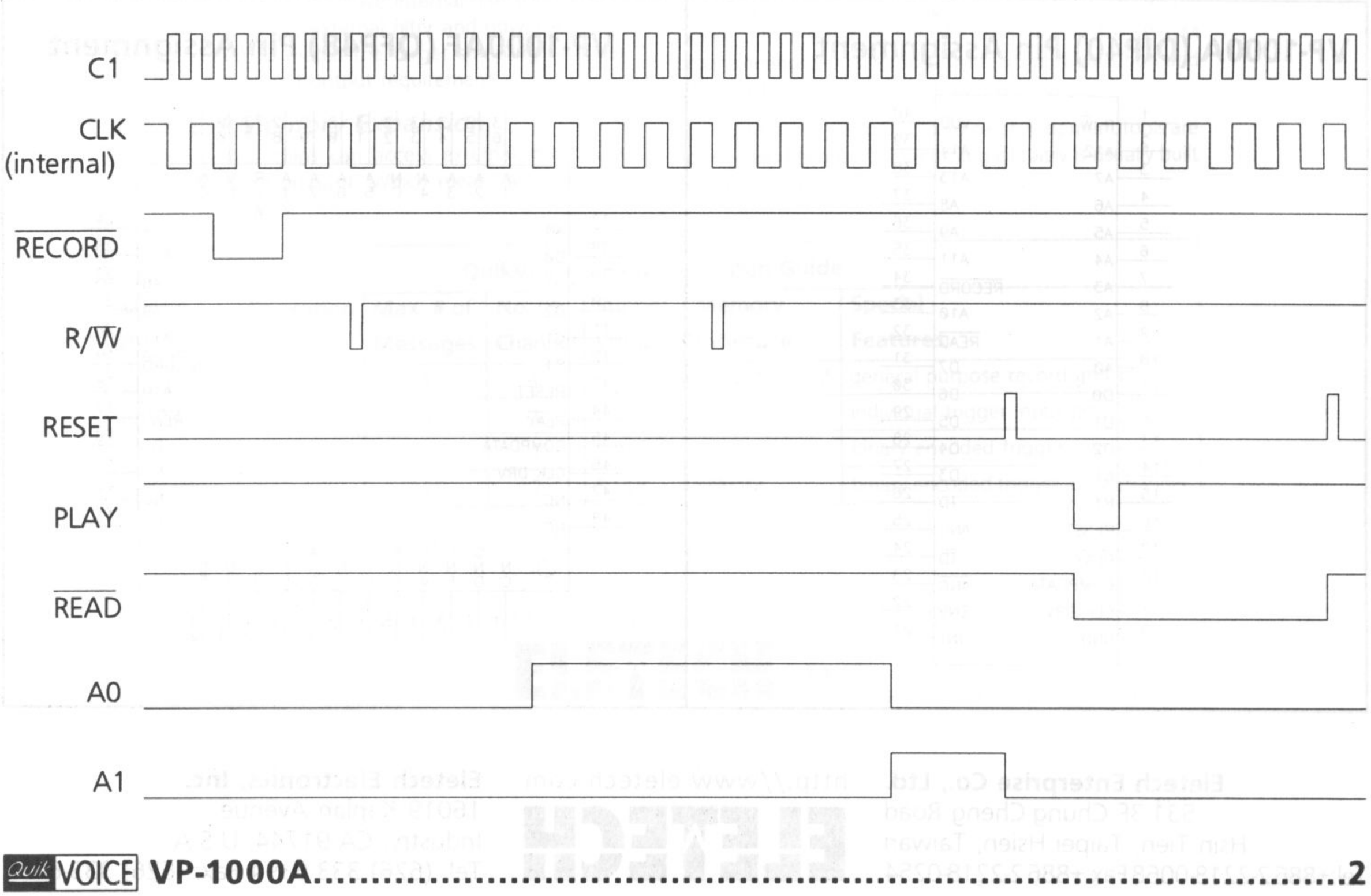
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, F_{OSC} = 64KHz, F_{CLOCK} = 32 KHz unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DD}	Standby Current			50		uA
I_{DRIVE}	Clock Drive Current		16			mA
I_{SINK}	Clock Sink Current		16			mA
V_{IH}	Input	High	3.5		5	V
V_{IL}	Voltage	Low	0		1.5	V
I_{DRIVE}	Output	Drive	3	4		mA
I_{SINK}	Current	Sink	3	4		mA
T_{RESET}	Reset Pulse Width		500			ns
T_{WRITE}	Write Pulse Width		200			ns
S/N	Signal-to-Quantizied Noise Ratio			30		dB

TIMING DIAGRAM



PIN DESCRIPTIONS

A0 - A14
Output, address bus, expandable by adding a counter.

ANG & $\overline{\text{ANG}}$
Output, differential analog audio signal.

C1
Input, internal RC oscillator. If external clock is to be used, it must be connected to this pin and its frequency twice as fast as the sampling rate.

CLK DRV
Output, a square wave of the same frequency as the sampling rate when the chip is in the Record or the Play mode. The frequency will be lower when the chip is in the Idle mode.

COMPDATA
Input, feedback from the external comparator output.

D0 - D7
Input/output, data bus.

ENV
Input, to be connected to an external integrator output.

INT
Output, connected to an external integrator to produce envelope waveform.

GND
Ground.

$\overline{\text{PLAY}}$
Input, active low. When the chip is idle but not under reset, pulsing this pin will put the chip in the Play mode.

R1
Output, internal RC oscillator. Leave un-connected when using external clock.

$\overline{\text{READ}}$
Output, active low. It indicates the chip is in the Play mode. This signal is usually used to enable memory output.

$\overline{\text{RECORD}}$
Input, active low. When the chip is idle but not under reset, pulsing this pin will put the chip in the Record mode.

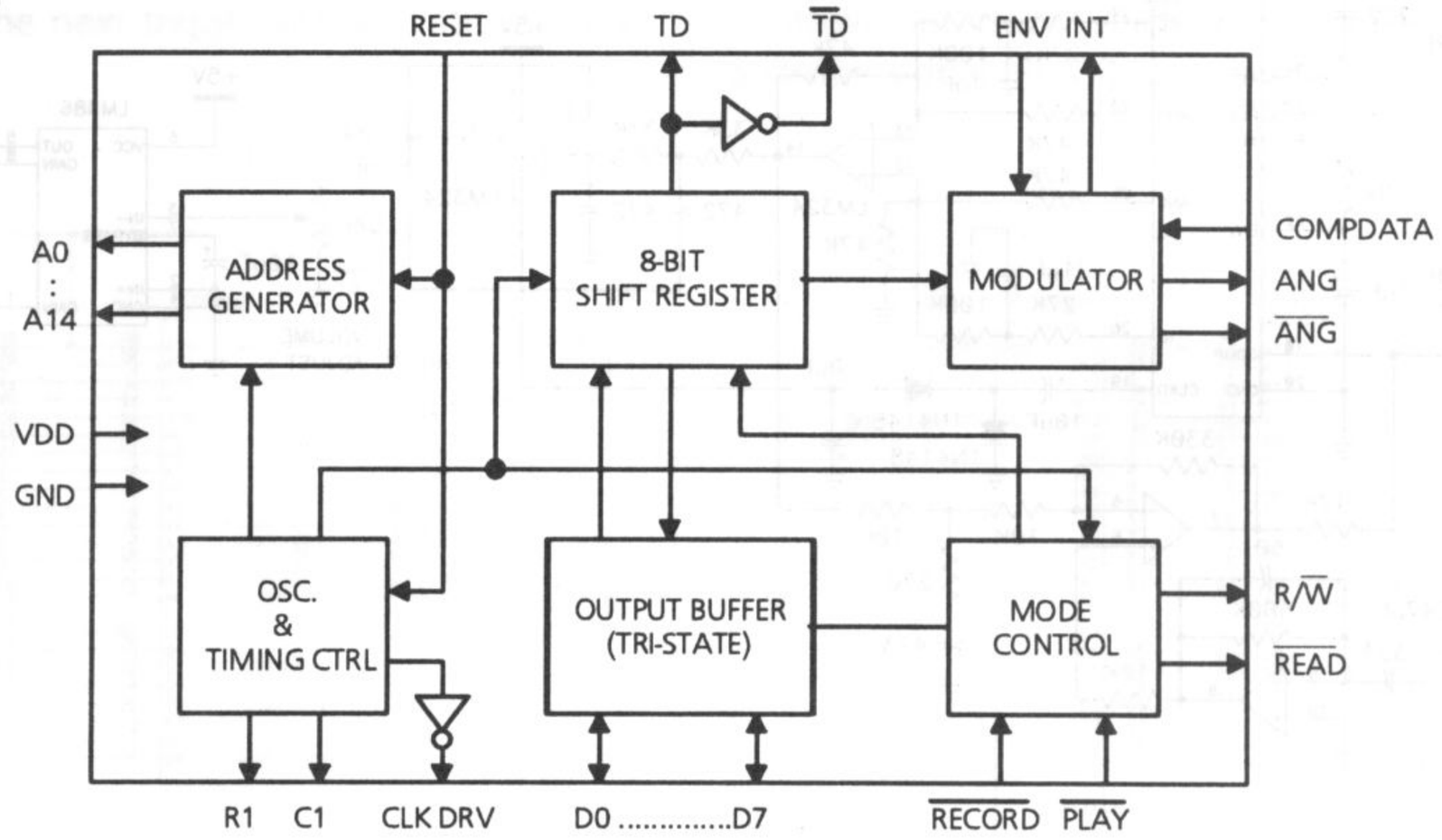
RESET
Input, active high. Reset the chip back to the Idle mode. This pin is level sensitive.

R/$\overline{\text{W}}$
Output, active low. This pin generates a pulse each time the clock counts to eight. It is usually used as a write strobe for the SRAM. Active only in the Record mode.

TD, $\overline{\text{TD}}$
Output, for signal modulation. These pins are useful in the Record mode only.

VDD
Input, supply voltage.

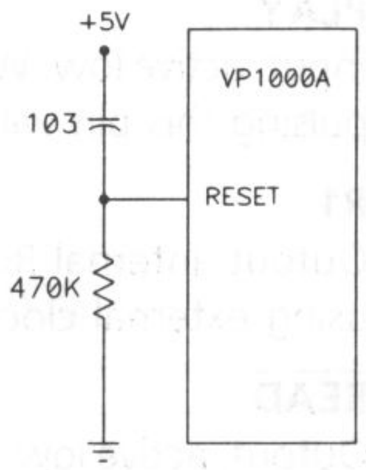
Block Diagram



APPLICATION NOTES

1. Reset Consideration

The Reset pin should never be left floating. If the Reset pin is not controlled by a non-floating signal, use the following Reset circuitry. Note that the 0.01uF capacitor is added so that the VP-1000A gets a Reset pulse on power-up.



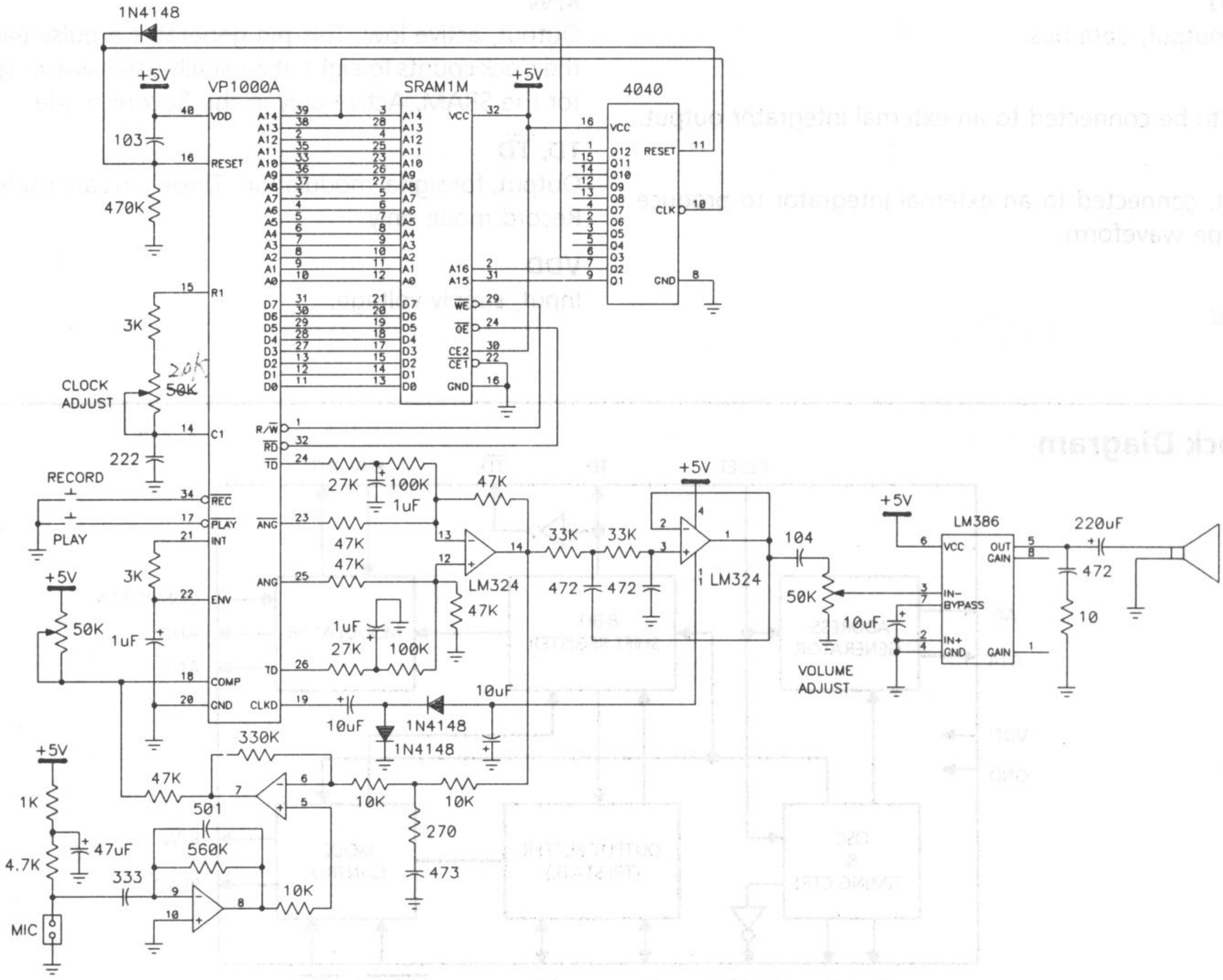
RECOMMENDED VP1000A RESET CIRCUITRY

2. Memory Address Expansion

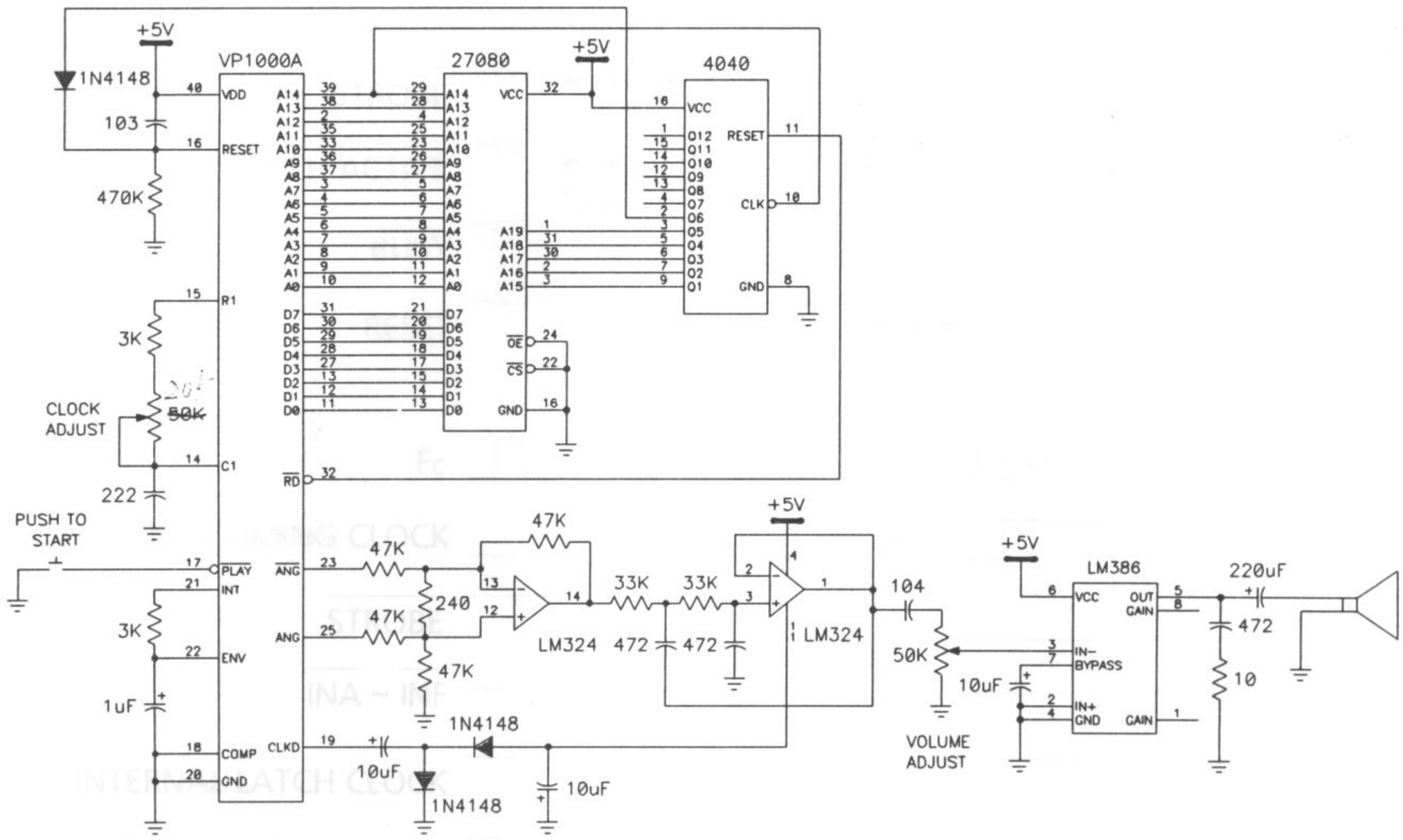
The VP-1000A's internal 15-bit address counter covers memory space up to 32K x 8, or 256K bits. It can be easily expanded by just adding a binary counter, clocked by the falling edge of address line A14. The first counter output becomes A15, the second output becomes A16 and etc. This is possible since once started, the VP-1000A will not stop recording or playing until it is reset. When the internal counter reaches the maximum count, it simply overflows and restarts from zero again. Therefore the VP-1000A can access an unlimited amount of memory.

CIRCUIT DESIGN EXAMPLES

1. Single-Message Record and Play, 1M SRAM

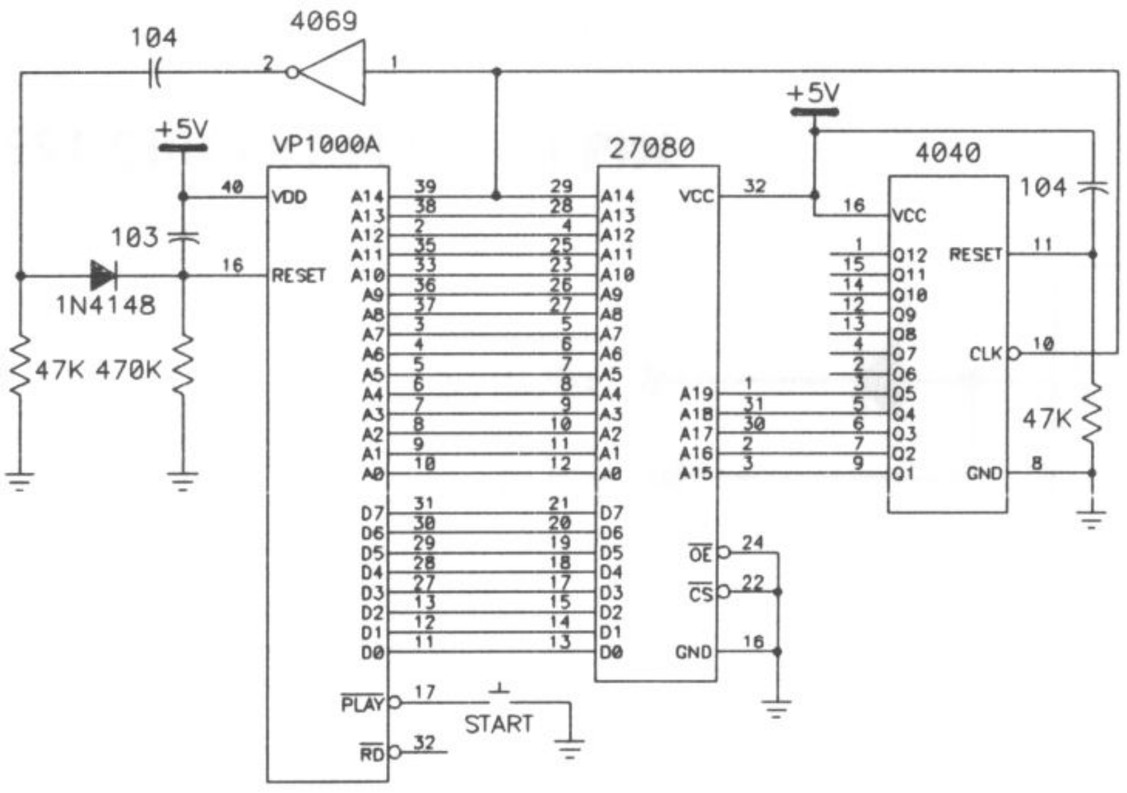


2. Single-Message Playback, 8M EPROM



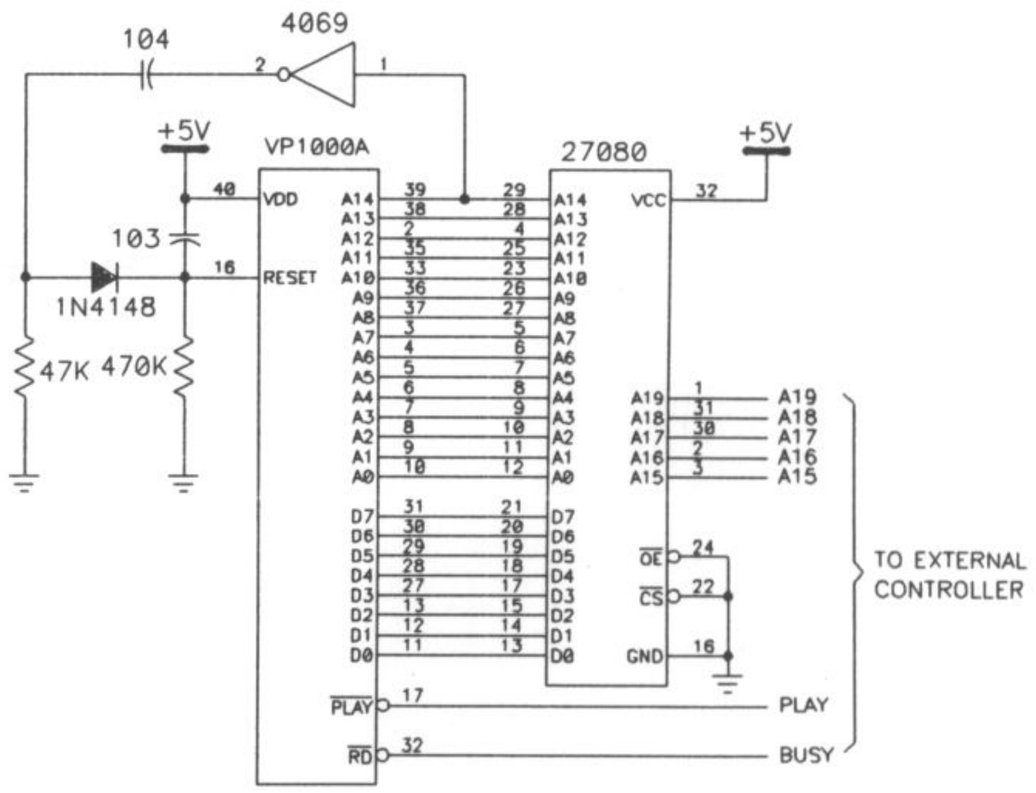
3. Multiple-Message Playback, Sequential Control

The 8M EPROM is divided into 32 equal segments of 256K bits. Each message is stored in such a segment and must be 256K bits or smaller. The first trigger will activate only the first segment. The next trigger will activate the next segment, and etc.



4. Multiple-Message Playback, Controller Interface

The 8M EPROM is divided into 32 equal segments of 256K bits. Each message is stored in such a segment and must be 256K bits or smaller. The message is activated via a controller interface which consists of 5 address lines and a strobe signal (PLAY).



Quik VOICE

VP-1410A
Digital Voice Processor

FEATURES

- High quality voice & sound generation
- 10 messages with direct trigger pins
- Playback-only with external EPROM or ROM
- Stand-alone operation
- 128K x 8 direct memory addressing, expandable
- Single 5V DC supply voltage
- Low power consumption
- Internal RC oscillator or external clock
- Continuous Variable Slope Delta (CVSD) modulation
- Sampling rate from 24Kbps to 128 Kbps
- Message digitization with the VP-880 system
- 48-pin DIP (VP-1410A) or 48-pin QFP (VP-1410AF)

GENERAL DESCRIPTIONS

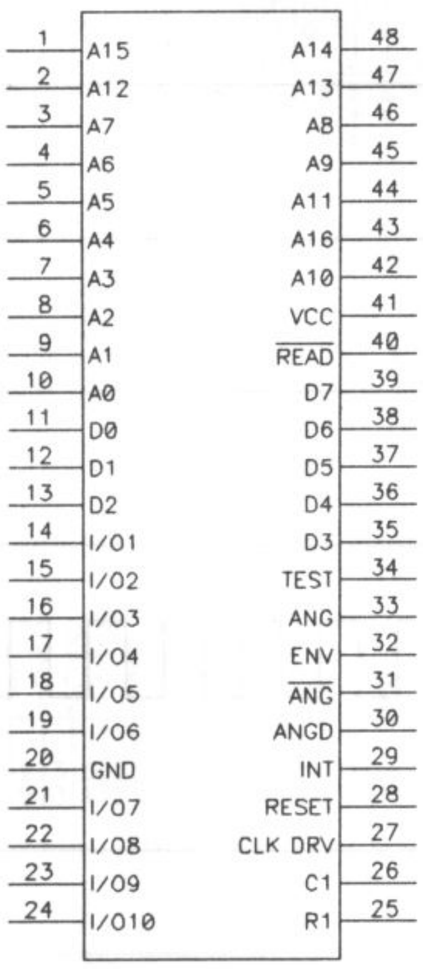
The VP-1410A Digital Voice Processor is an advanced CMOS LSI chip designed for multiple-message playback applications. It can access up to 10 different messages of variable length stored in external EPROM or ROM chips. Message activation is simplified since each message has its own trigger pin . If memory bank switching technique is used, the number of messages supported can be easily expanded to 20, 40 or more.

The VP-1410A is totally self-contained. It can access the external memory all by itself without the help from any microprocessor. Although the chip provides only 16 address lines, an external counter can be easily added to extend the memory addressing to virtuely no limitation. Therefore very long message length can be achieved easily. Overall, the VP-1410A offers high voice quality and flexible memory addressing that no other chips can.

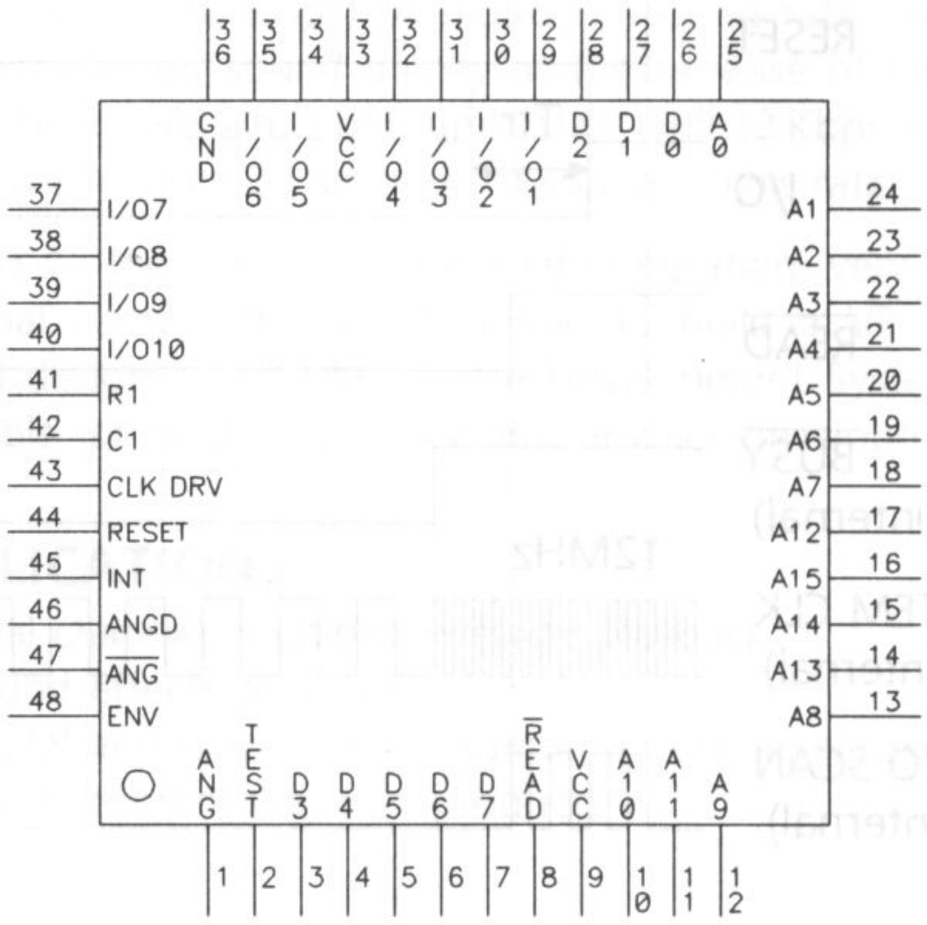
APPLICATIONS

- Multiple message playback
- Sound effects generator
- Digital message repeaters for consumer, industrial, security and telecommunication products

VP-1410A (DIP48) Pin Assignment



VP-1410AF (QFP48) Pin Assignment



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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, V_{DD} - V_{SS} ..... 0 to 5.5V
Input Volotage, V_{IN} ..... V_{SS} to V_{DD}
Operating Temperature, T_{OP} ..... -10°C to 60°C
Storage Temperature, T_{ST} ..... -20°C to 80°C

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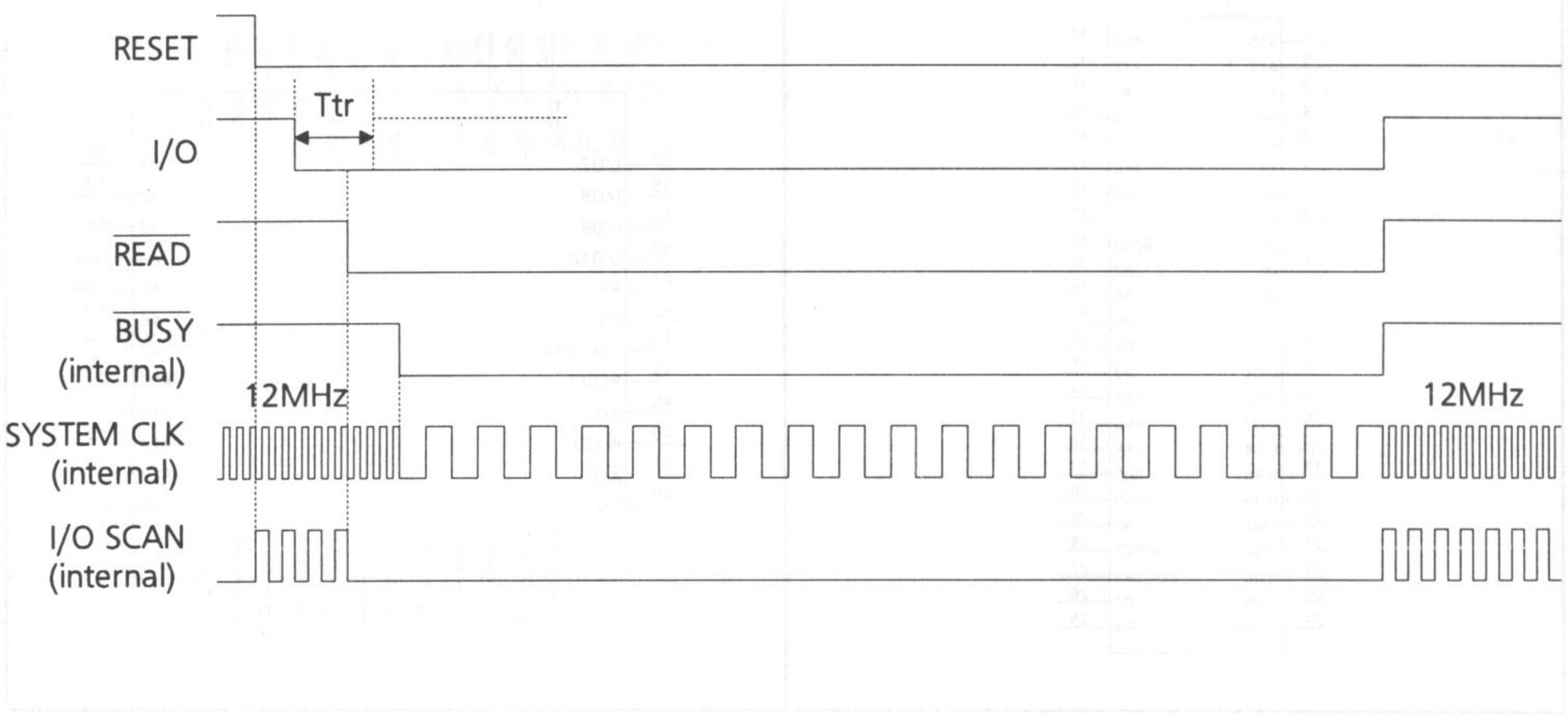
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, F_{OSC} = 2048KHz, F_{CLOCK} = 32 KHz unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DD}	Standby Current			1.4		mA
I_{DRIVE}	Clock Drive Current		12			mA
I_{SINK}	Clock Sink Current		12			mA
V_{IH}	Input	High	3.5		5	V
V_{IL}	Voltage	Low	0		1.5	V
I_{DRIVE}	Output	Drive	3	4		mA
I_{SINK}	Current	Sink	3	4		mA
T_{RESET}	Reset Pulse Width		500			ns
T_{tr}	I/O Input Pulse Width			35		us
F_C	Internal Memory Search Clock			12		MHz

TIMING DIAGRAM



PIN DESCRIPTIONS

A0 - A16
Output, address bus, expandable by adding a counter. Note that VP-1410AF does not have A16.

ANG & $\overline{\text{ANG}}$
Output, differential analog audio signal.

ANGD
Input, analog signal to be connected to the external comparator output.

C1
Input, internal RC oscillator. If external clock is to be used, it must be connected to this pin and its frequency 64x the sampling rate.

CLK DRV
Output, buffered clock signal, a square wave of the same frequency as the sampling rate.

D0 - D7
Input, data bus.

ENV
Input, to be connected to an external integrator output.

INT
Output, connected to an external integrator to produce envelope waveform.

GND
Ground.

I/O1 ~ I/O10
Input/output, trigger pin, active low. I/O1 is for message #1, I/O2 is for message #2 and etc. When the chip is idle but not under reset, this pin is the trigger input and pulsing it will put the chip in the "Play" mode and start the message. Once in the "Play" mode, the pin becomes a "low" output until the message is over.

R1
Output, internal oscillator pin. Leave un-connected when using external clock.

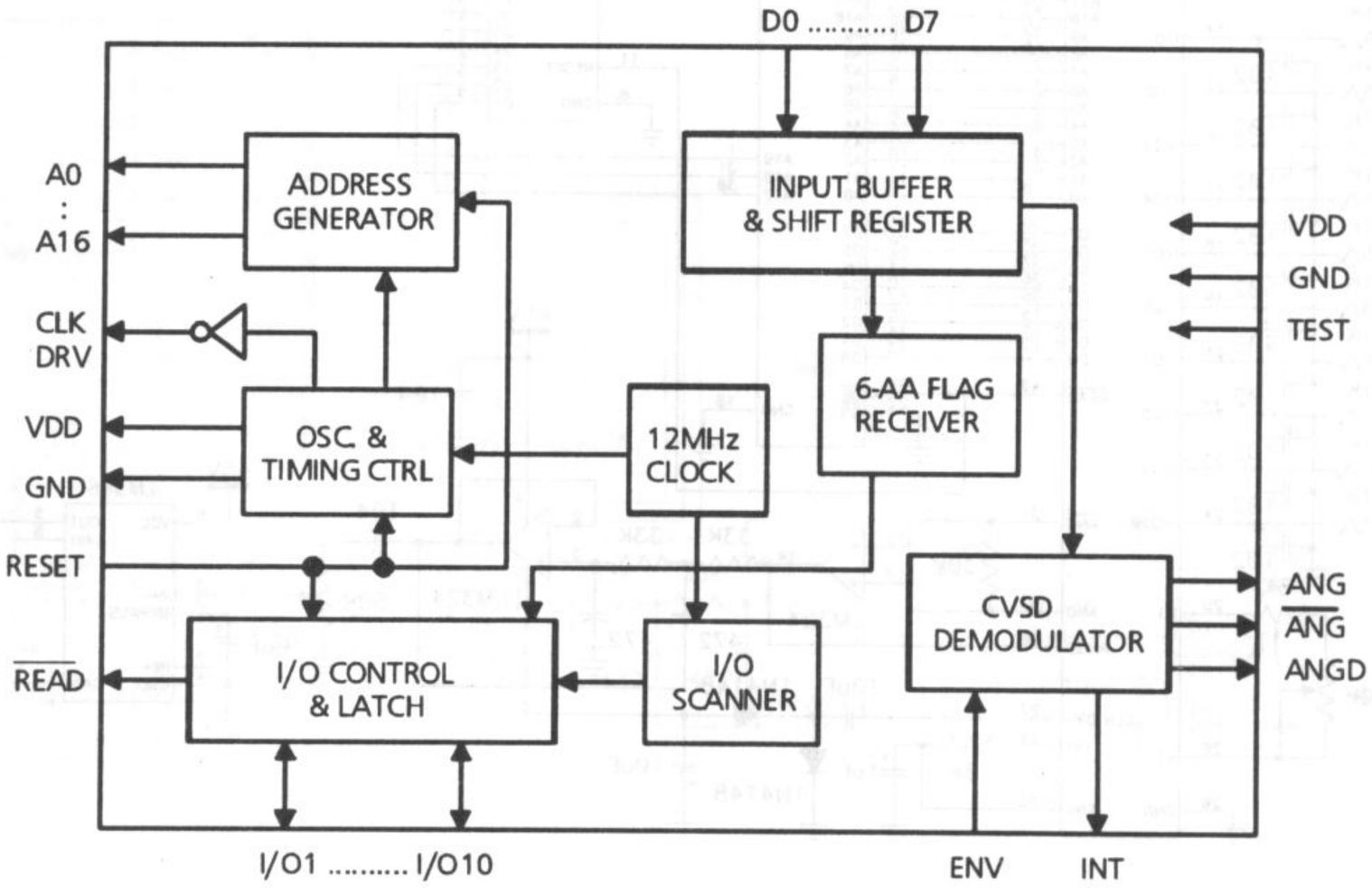
$\overline{\text{READ}}$
Output, active low. It indicates the chip is in the "Play" mode. This signal is usually used to enable memory output.

RESET
Input, active high. Reset the chip back to the "Idle" mode. This pin is level sensitive.

TEST
For factory use only, keep it un-connected.

VCC
Input, supply voltage.

Block Diagram



APPLICATION NOTES

1. VP-1410AF Missing A16

Due to packaging constraint, the VP-1410AF does not provide address line A16. Therefore, A16 must be generated externally by adding a binary counter, as explained below.

2. Memory Address Expansion

The VP-1410A's internal 17-bit address counter covers memory space up to 128K x 8, or 1M bits. It can be easily expanded by just adding an external binary counter, clocked by the falling edge of address line A16. The first counter output becomes A17, the second output becomes A18 and etc. This is possible since once started, the VP-1410A will continue to play until it reaches the EOM (End Of Message) flag. When the internal address counter reaches the maximum count before the chip sees the EOM flag, the counter simply overflows and restarts from zero again. Therefore the VP-1410A can access an unlimited amount of memory by adding an external address counter.

3. EOM (End Of Message) Flag

The EOM flag consists of six consecutive bytes of "AA", or "10101010" in binary format. After a trigger signal is received, the VP-1410A uses the internal 12MHz system clock to scan through memory space and finds the correct message by counting the number of EOM flags. For example, to find the 5th message, it must scan through each and every memory location until it finds 4 EOM flags. The first byte following the 4th EOM flag is the first byte of the 5th message.

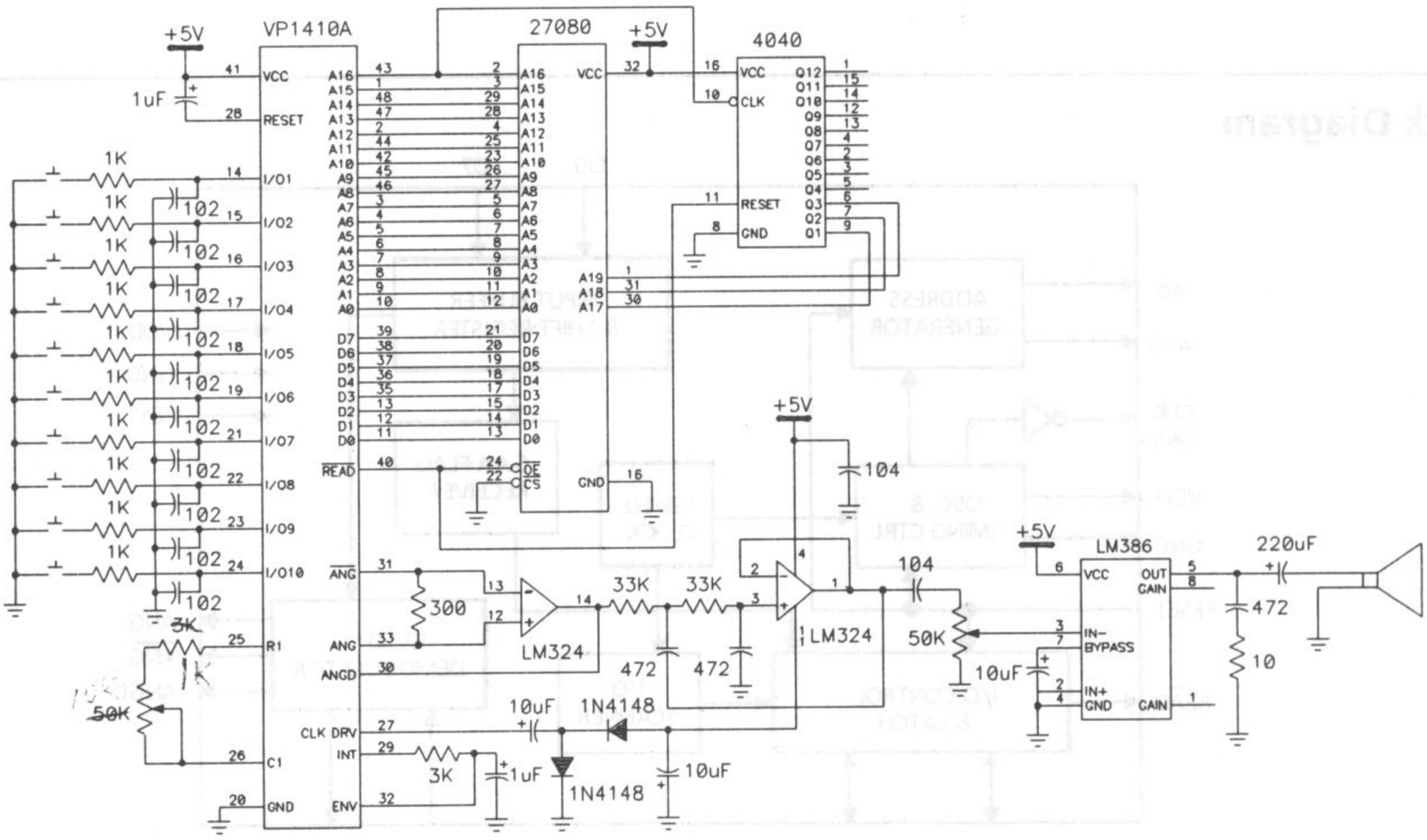
4. Creating Master EPROM File on the VP-880 System

Follow these steps to create the master EPROM file:

1. Digitize, edit and save each message in a separate file.
2. Use VP-880's function "H" to combine all the messages together. The VP-880 program will automatically search and eliminate any EOM flag within each messge, which is naturally formed during digitization. It will then put a EOM flag at the end of each message and combine them into one or several master files.

CIRCUIT DESIGN EXAMPLES

1. 10-Message Playback, 8M EPROM



Quik VOICE

VP-1606
Digital Voice Processor

FEATURES

- Plays messages stored in external EPROM chips
- CVSD technique with adjustable sampling rate from 16K to 128K bps for different voice quality
- Direct access to 64 segments, more segments are possible with external decoding circuitry
- Built-in RC oscillator or use external clock
- Direct EPROM addressing up to 8M bits, easy memory expansion with external bank switching
- Low power, single voltage operation
- Microprocessor interface
- Low-cost VP-880 system available for quick and easy voice development

GENERAL DESCRIPTIONS

The VP-1606 is a CMOS LSI speech processor chip based on the CVSD (Continuously Variable Slope Delta) modulation technique. The VP-1606 is designed to replace the combination of the VP1000 and the VP1600. It also provides extended direct EPROM addressing (up to 8M bits), with possible expansion.

The VP1606 can randomly access and play back up to 64 sound segments (or messages) stored in 4 EPROM banks, with up to 16 segments in each bank.

Each segment stored in the EPROM is represented by a unique binary code: 2 bits for the bank code and 4 bits for the segment code. A valid code plus a strobe signal are all it takes to activate a certain segment.

The VP-1606 can operate within a wide range of sampling rates (from 16 to 128 Kbps). A higher sampling rate usually produces a better sound quality at the expense of higher memory cost. As a rule of thumb, start with the standard 32 Kbps rate. A 1M EPROM can store 32 seconds of sound at this rate.

Thanks to the chip's high internal integration, very little external components are required to build a VP-1606 based design. Also, the VP880 Voice Development System is available for quick and easy in-house voice development and programming. Therefore the VP-1606 is an ideal choice for both high-end and low-end applications.

VP-1606 (DIP48) Pin Assignment

APPLICATIONS

- Voice memo recorder
- Sound effects generator
- Digital announcer for consumer, industrial, security and telecommunication products

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ABSOLUTE MAXIMUM RATINGS*

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Input Volotage, V_{IN} ..... V_{DS} to V_{CC}
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Storage Temperature, T_{ST} ..... -20°C to 80°C

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ELECTRICAL CHARACTERISTICS

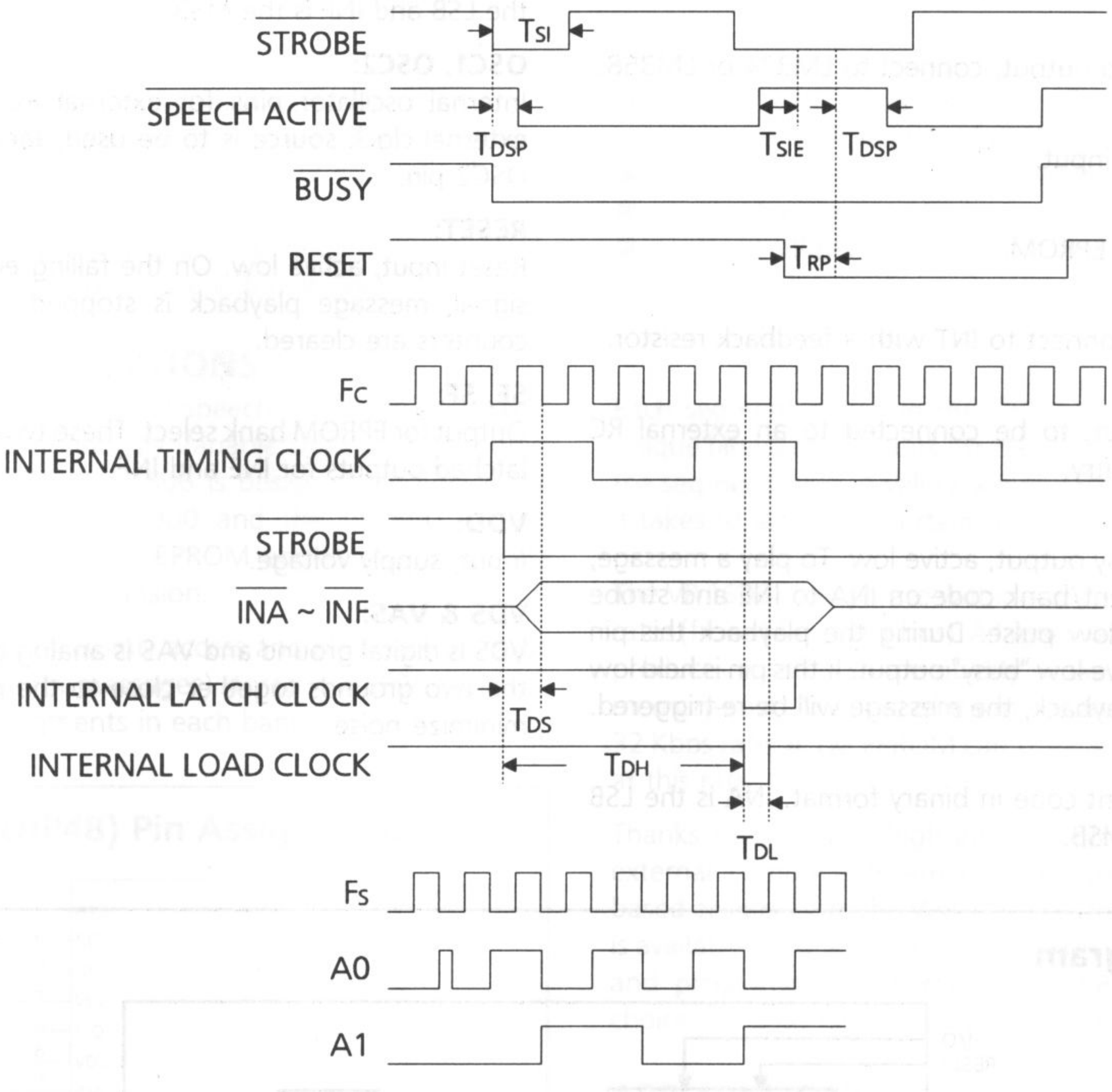
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
I_{DD}	Standby Current		50		uA
I_{DRIVE}	Output Current V_{OH}=2.4V		4		mA
I_{SINK}	Output Current V_{OL}=0.4V		4		mA
V_{IH}	Input Voltage (High)		3.5		V
V_{IL}	Input Voltage (Low)		1.5		V
F_C	Internal Scan Clock		8		MHz
F_S	Sampling Clock	20	32	128	KHz
T_{RESET}	Reset Pulse Width		1		us
T_{SI}	Strobe Input Pulse Width		1		us
T_{SIE}	Strobe Inhibit Time After EOS (1)		1.5		ms
T_{DSP}	Delay Time From Strobe To Play (2)			150	ms
T_{RP}	Edge-Triggered Reset Interval		1		us
T_{DS}	Data Setup Time For INA ~ INF			350	ns
T_{DH}	Data Hold Time For INA ~ INF		1		us
T_{DL}	Internal Load Pulse For INA ~ INF		65		ns

Note:

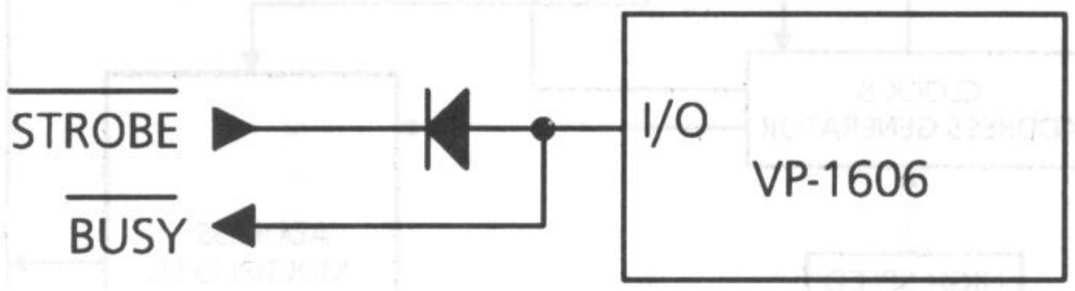
(1) EOS = End-Of-Speech

(2) Based on 1M EPROM scanning.

TIMING DIAGRAM



TEST CIRCUIT FOR I/O PIN



PIN DESCRIPTIONS

A0 ~ A19:
Address output to EPROM.

ANG & ANG\:
Differential audio output, connect to LM324 or LM358.

ANGD:
Audio feedback input.

D0 ~ D7:
Data input from EPROM.

ENV:
Envelop input, connect to INT with a feedback resistor.

INT:
Integrator output, to be connected to an external RC integration circuitry.

I/O:
Strobe input/Busy output, active low. To play a message, place the segment/bank code on INA to INE and strobe this pin with a low pulse. During the playback this pin becomes an active-low "busy" output. If this pin is held low at the end of playback, the message will be re-triggered.

INA ~ IND:
Input for segment code in binary format. INA is the LSB and IND is the MSB.

INE, INF:
Input for bank code in binary format, max. 4 banks. INE is the LSB and INF is the MSB.

OSC1, OSC2:
Internal oscillator pins for external RC components. It external clock source is to be used, feed it through the OSC2 pin.

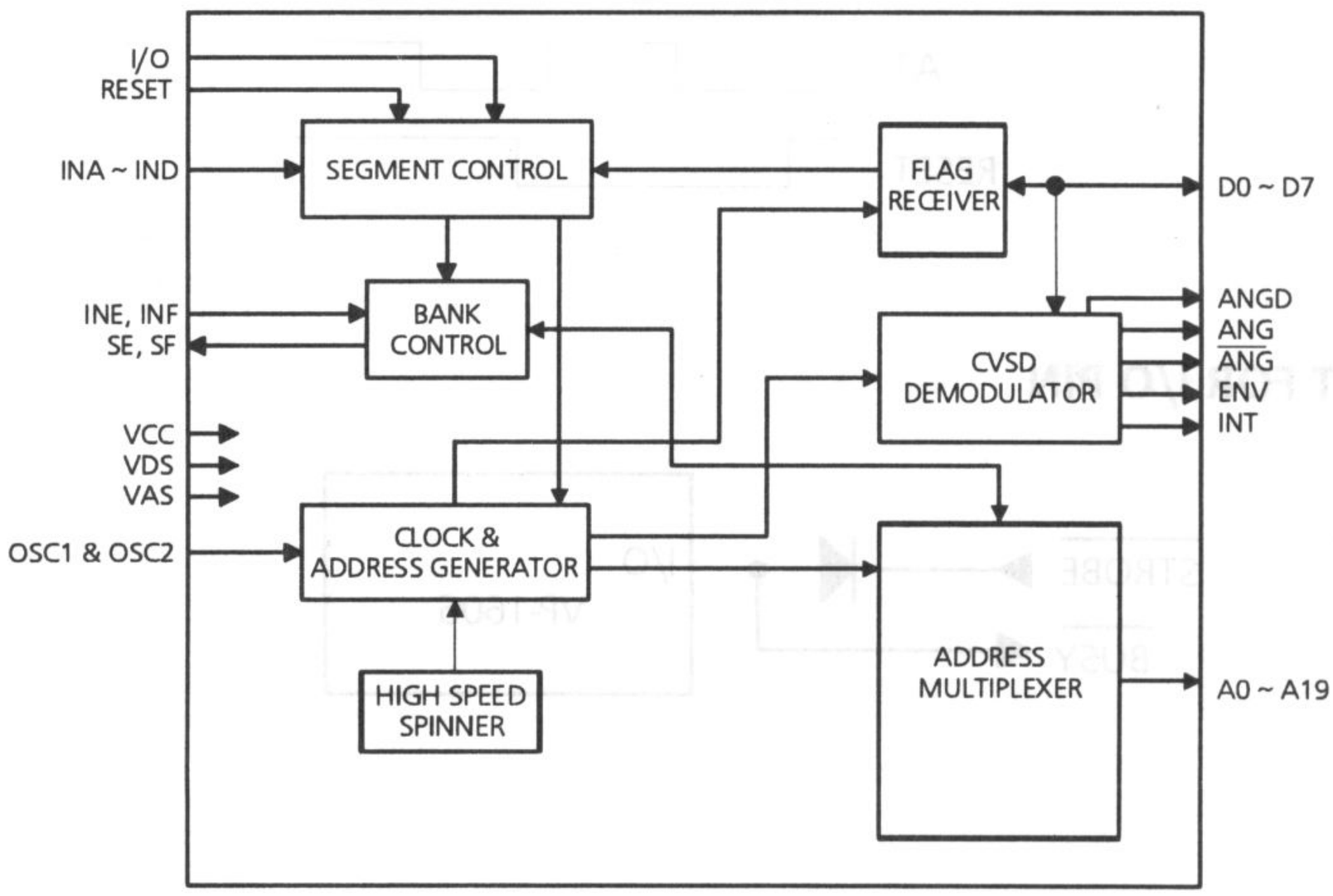
RESET:
Reset input, active low. On the falling edge of this reset signal, message playback is stopped and all internal counters are cleared.

SE, SF:
Output for EPROM bank select. These two pins are actually latched outputs for INE and INF.

VDD:
Input, supply voltage.

VDS & VAS:
VDS is digital ground and VAS is analog ground. Connect the two grounds together close to the power source to minimize noise.

Block Diagram



APPLICATION NOTES

1. EOM (End Of Message) Flag

The EOM flag consists of six consecutive bytes of "AA", or "10101010" in binary format. After a trigger signal is received, the VP-1606 uses the internal 8MHz system clock to scan through memory space and finds the correct message by counting the number of EOM flags. For example, to find the 5th message, it must scan through each and every memory location until it finds 4 EOM flags. The first byte following the 4th EOM flag is the first byte of the 5th message.

2. Creating Master EPROM File on the VP-880 System

Follow these steps to create the master EPROM file:

1. To maximize the EPROM usage, arrange your sound segments in banks of 16 or less, so that the total combined length for each bank is about the same. Do not mix channel A and channel B together.

2. Based on the total combined length of the largest bank, select a highest sampling rate that will fully utilize the EPROM. Use the following equation:

Sampling Rate (Kbps) =
EPROM Size (K-bits) / Total Length (Second)

3. Digitize and edit each segment as a separate file. Use the "ROM Data Management" function to combine up to 16 messages into a "bank file". The first filename entered in the "ROM Data Management" is the first segment in that bank, and etc.

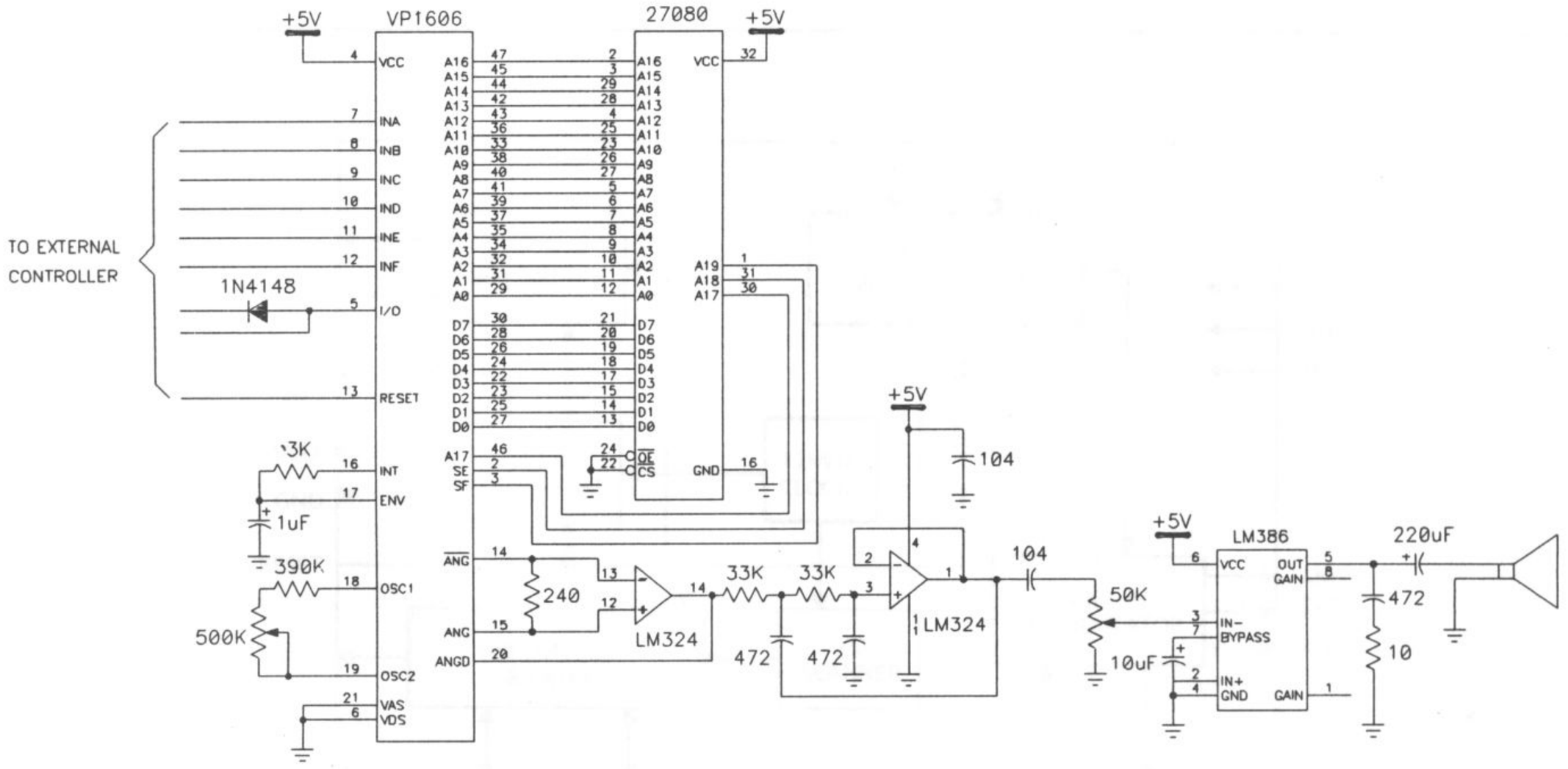
4. Depending on the hardware design, each EPROM chip may contain one or more sound banks. If you need to combine several bank files into one for programming into one EPROM chip, use the following DOS command:

COPY /b file_1+file_2+..+file_n destination_file

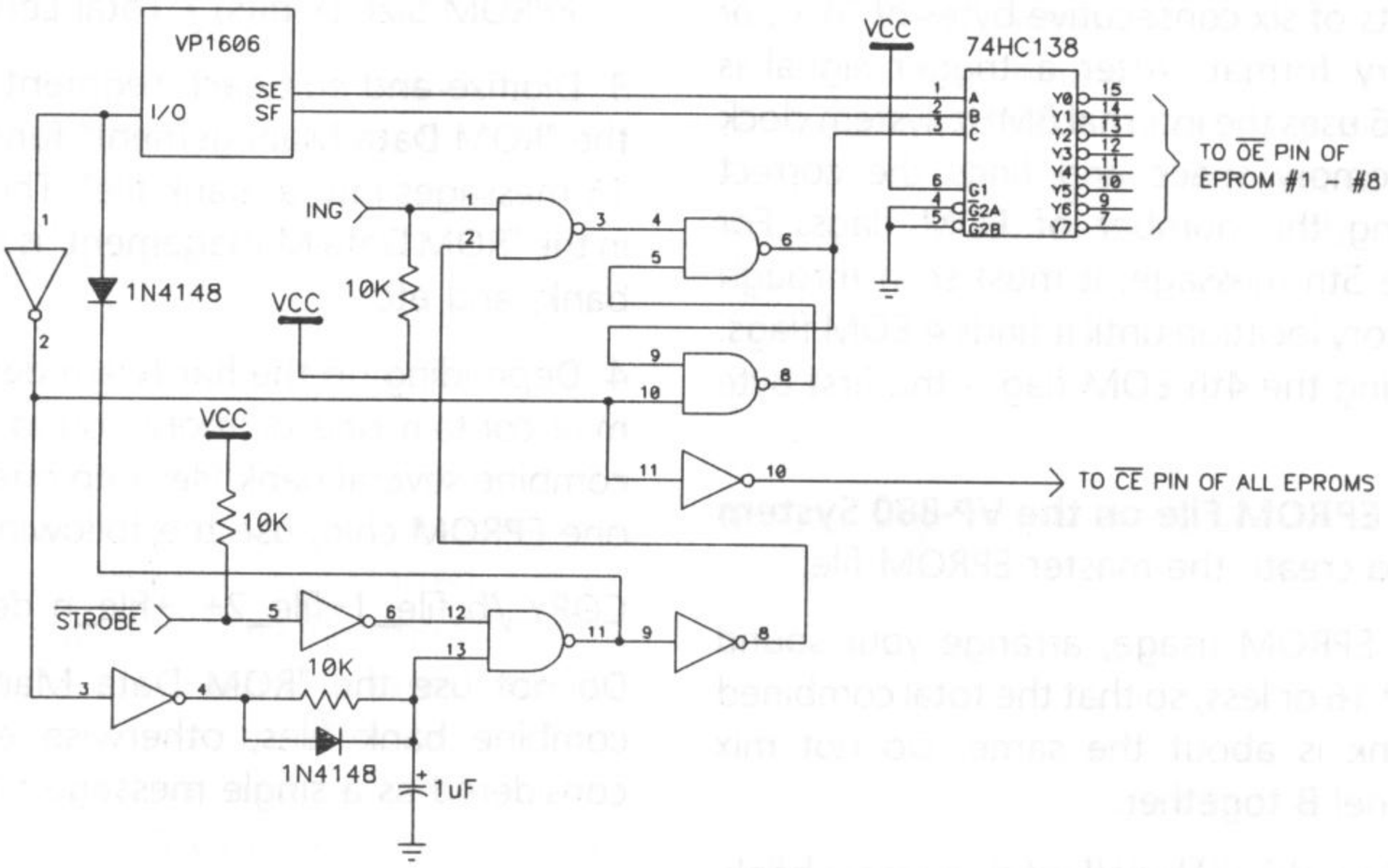
Do not use the "ROM Data Management" function to combine bank files, otherwise each bank file will be considered as a single message file.

CIRCUIT DESIGN EXAMPLES

1. 64-Message Playback, 8M EPROM, 2M Per Bank



2. Segment Expansion (128 Segments)



Quik VOICE

VP-1608
Digital Voice Processor

FEATURES

- Plays messages stored in external EPROM chips
- CVSD technique with adjustable sampling rate from 16K to 128K bps for different voice quality
- Dual-channel audio output
- Up to 64 segments per channel
- Built-in RC oscillator or use external clock
- Direct EPROM addressing up to 8M bits
- Low power, single voltage operation
- Microprocessor interface
- Low-cost VP-880 system available for quick and easy voice development

GENERAL DESCRIPTIONS

The VP-1608 is a CMOS LSI speech processor chip based on the CVSD (Continuously Variable Slope Delta) modulation technique. The VP-1608 not only combines the functions of the VP1000 and the VP1600 together, but also provides extended direct EPROM addressing (up to 8M bits) and dual-channel audio output.

Note that although the dual-channel output provided by the VP1608 can be used as a stereo output, it will be hard to do so since the VP-880 Voice Development System does not allow stereo voice digitization.

Therefore the dual-channel output is usually used in applications where sound synchronization is not critical. For example, in a game equipment, channel A can be playing a continuous background sound when channel B plays short sound effects based on the player's action.

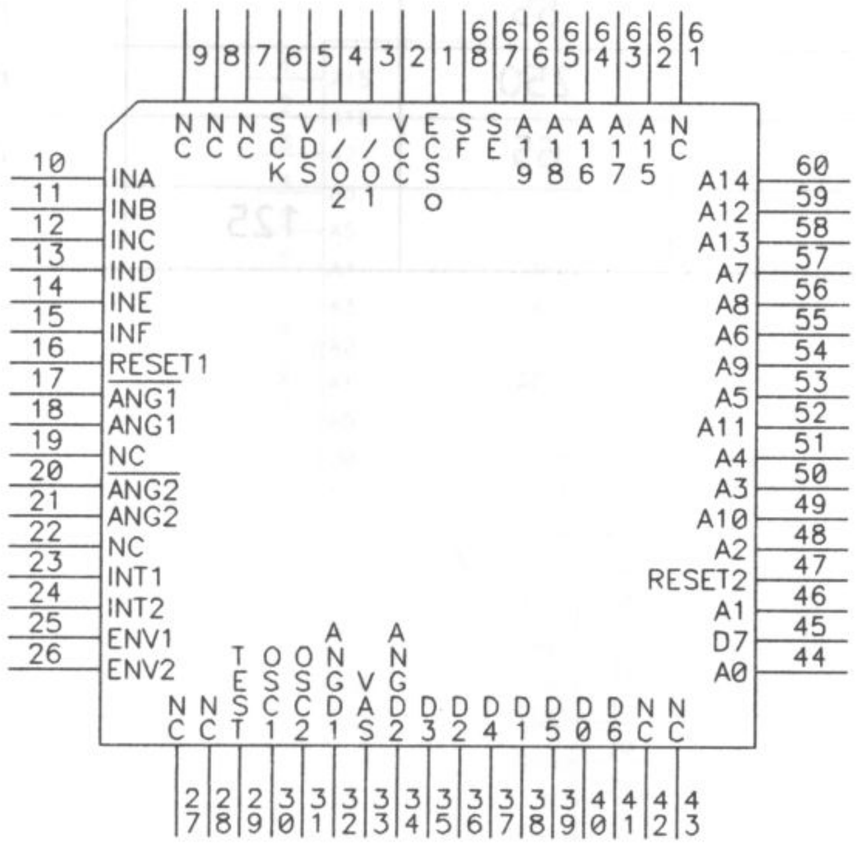
The dual-channel output is available on two separate output pins. They can be used independently, or mixed together externally. Each channel may control up to 64 sound segments stored in 4 different EPROM banks, with up to 16 segments in each bank.

Each segment stored in the EPROM is represented by a unique binary code: 2 bits for the bank code and 4 bits for the segment code. A valid code plus a strobe signal are all it takes to activate a certain segment.

The VP-1608 can operate in a wide range of sampling rates (from 16 to 128 Kbps). A higher sampling rate usually produces better sound quality at the expense of higher memory cost. As a rule of thumb, start with 32 Kbps. A 1M EPROM can store 32 seconds of sound at this rate.

Thanks to the chip's high internal integration, very little external components are required to build a VP-1608 based design. The VP880 Voice Development System is available for quick and easy in-house voice development.

VP-1608 (PLCC68) Pin Assignment



APPLICATIONS

- Dual channel, multiple message playback
- Sound effects generator
- Digital announcer for consumer, industrial, security and telecommunication products

Eletech Enterprise Co., Ltd.
531-3F Chung-Cheng Road
Hsin Tien, Taipei Hsien, Taiwan
Tel:+886 2-2218-0068 Fax:+886 2-2218-0254

http://www.eletech.com

ELETECH

Eletech Electronics, Inc.
16019 Kaplan Avenue
Industry, CA 91744, U.S.A.
Tel: (626) 333-6394 Fax: (626) 333-6494

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, V_{CC} - V_{DS} ..... 0 to 5.5V
Input Volotage, V_{IN} ..... V_{DS} to V_{CC}
Operating Temperature, T_{OP} ..... -10°C to 60°C
Storage Temperature, T_{ST} ..... -20°C to 80°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

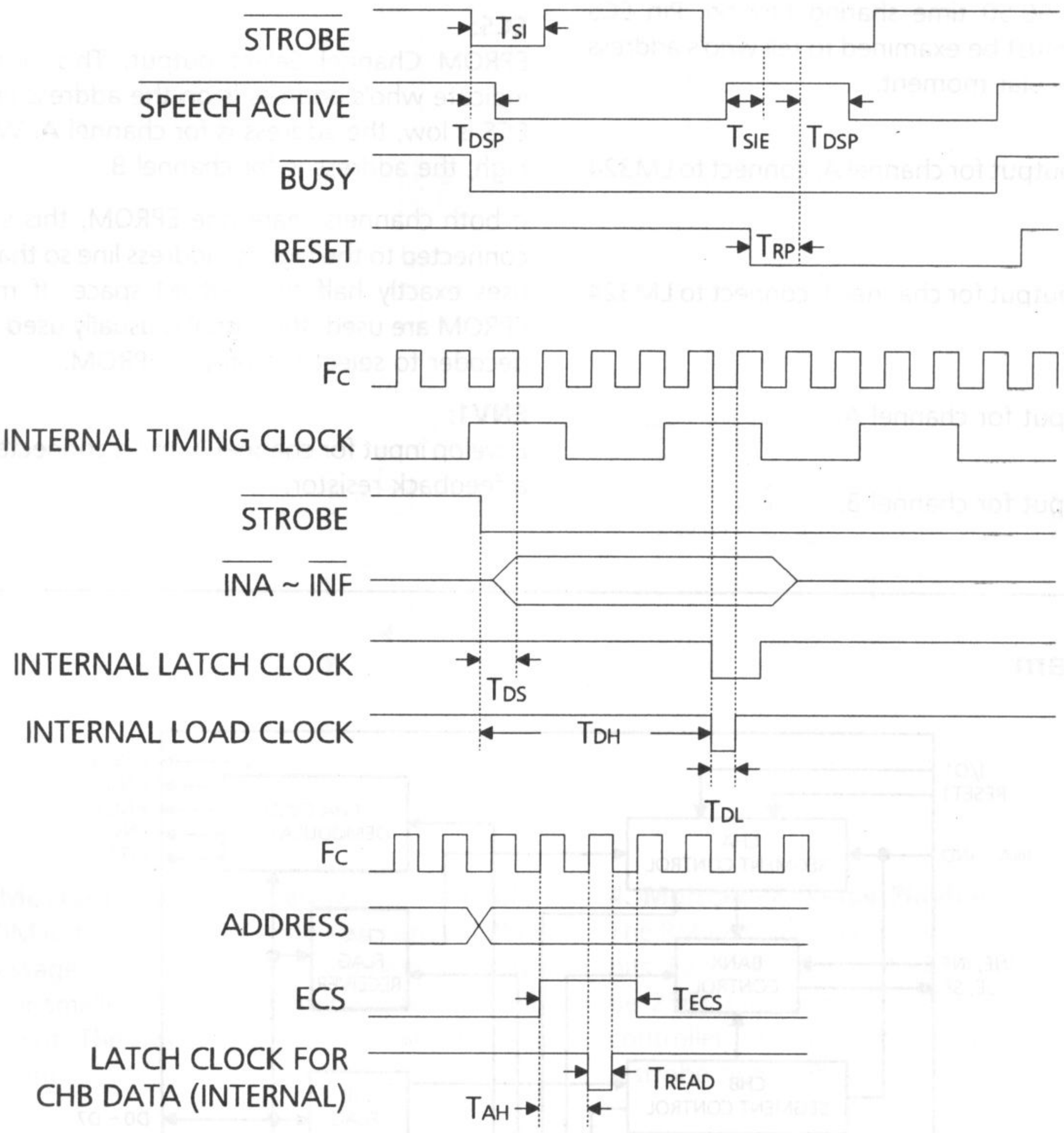
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
I_{DD}	Standby Current		50		uA
I_{DRIVE}	Output Current V_{OH}=2.4V		4		mA
I_{SINK}	Output Current V_{OL}=0.4V		4		mA
V_{IH}	Input Voltage (High)		3.5		V
V_{IL}	Input Voltage (Low)		1.5		V
F_C	Internal Scan Clock		8		MHz
F_S	Sampling Clock	20	32	128	KHz
T_{RESET}	Reset Pulse Width		1		us
T_{SI}	Strobe Input Pulse Width		1		us
T_{SIE}	Strobe Inhibit Time After EOS (1)		1.5		ms
T_{DSP}	Delay Time From Strobe To Play (2)			150	ms
T_{RP}	Edge-Triggered Reset Interval		1		us
T_{DS}	Data Setup Time For INA ~ INF			350	ns
T_{DH}	Data Hold Time For INA ~ INF		1		us
T_{DL}	Internal Load Pulse For INA ~ INF		65		ns
T_{ECS}	Address Valid Time For Ch. B EPROM		250		ns
T_{READ}	Internal Latch Pulse For Ch. B EPROM Data		65		ns
T_{AH}	Address Stable Time For Ch. B			125	ns

Note:

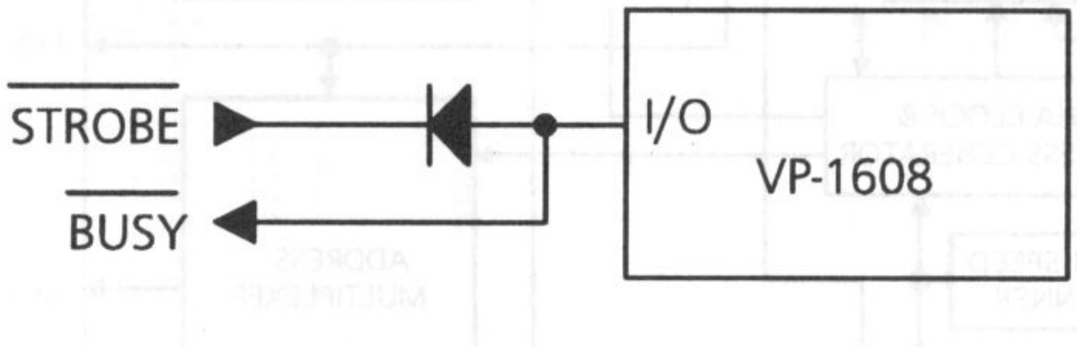
(1) EOS = End-Of-Speech

(2) Based on 1M EPROM scanning.

TIMING DIAGRAM



TEST CIRCUIT FOR I/O PIN



PIN DESCRIPTIONS

A0 ~ A19:
Address output to EPROM. Both channels share the same address lines in a 50-50 time sharing fashion. Pin ECS (described below) must be examined to tell who's address is valid at any particular moment.

ANG1 & ANG1\:
Differential audio output for channel A, connect to LM324 or LM358.

ANG2 & ANG2\:
Differential audio output for channel B, connect to LM324 or LM358.

ANGD1:
Audio feedback input for channel A.

ANGD2:
Audio feedback input for channel B.

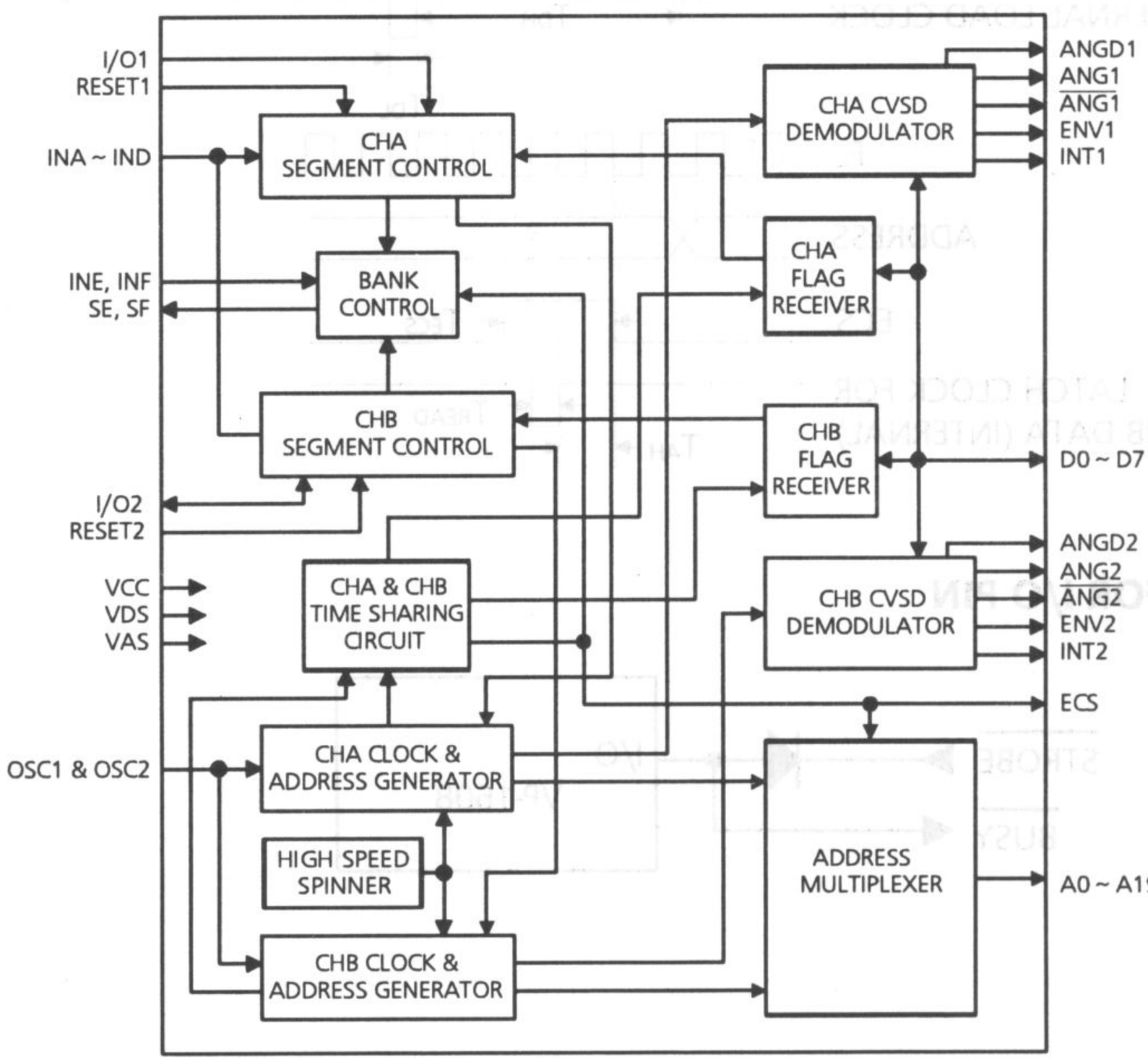
D0 ~ D7:
Data input from EPROM.

ECS:
EPROM Channel Select output. This signal is used to indicate who's address is on the address lines. When the ECS is low, the address is for channel A. When the ECS is high, the address is for channel B.

If both channels share one EPROM, this signal is usually connected to the highest address line so that each channel uses exactly half the EPROM space. If more than one EPROM are used, this signal is usually used by the address decoder to select the proper EPROM.

ENV1:
Envelop input for channel A, to be connected to INT1 with a feedback resistor.

Block Diagram



ENV2:
Envelop input for channel B, to be connected to INT2 with a feedback resistor.

INT1:
Integrator output for channel A, to be connected to an external RC integration circuitry.

INT2:
Integrator output for channel B, to be connected to an external RC integration circuitry.

I/O1:
Strobe input/Busy output for channel A, active low. To play a message on channel A, place the segment/bank code on INA to INE and strobe this pin with a low pulse. During the playback this pin becomes an active-low "busy" output. If this pin is held low at the end of playback, the message will be re-triggered.

I/O2:
Same as I/O1 except that this pin is for channel B.

INA ~ IND:
Input for segment code in binary format. INA is the LSB and IND is the MSB.

INE, INF:
Input for bank code in binary format, max. 4 banks. INE is the LSB and INF is the MSB.

OSC1, OSC2:
Internal oscillator pins for external RC components. It external clock source is to be used, feed it through the OSC2 pin. Note that both channels share the same clock, so their sampling rate must be the same.

RESET1:
Reset input for channel A, active low. On the falling edge of this reset signal, channel A playback is stopped and all internal counters for channel A are cleared.

RESET2:
Reset input for channel B, active low. On the falling edge of this reset signal, channel B playback is stopped and all internal counters for channel B are cleared.

SCK, TEST:
For factory use only, do not make any connection.

SE, SF:
Output for EPROM bank select. These two pins are actually latched outputs for INE and INF.

VDD:
Input, supply voltage.

VDS & VAS:
VDS is digital ground and VAS is analog ground. Connect the two grounds together close to the power source to minimize noise.

APPLICATION NOTES

1. EOM (End Of Message) Flag

The EOM flag consists of six consecutive bytes of "AA", or "10101010" in binary format. After a trigger signal is received, the VP-1608 uses the internal 8MHz system clock to scan through memory space and finds the correct message by counting the number of EOM flags. For example, to find the 5th message, it must scan through each and every memory location until it finds 4 EOM flags. The first byte following the 4th EOM flag is the first byte of the 5th message.

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Follow these steps to create the master EPROM file:

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4. Depending on the hardware design, each EPROM chip may contain one or more sound banks. It is also possible to use just one EPROM to store all sound segments of both channel A and channel B. If you need to combine several bank files into one for programming into one EPROM chip, use the following DOS command:

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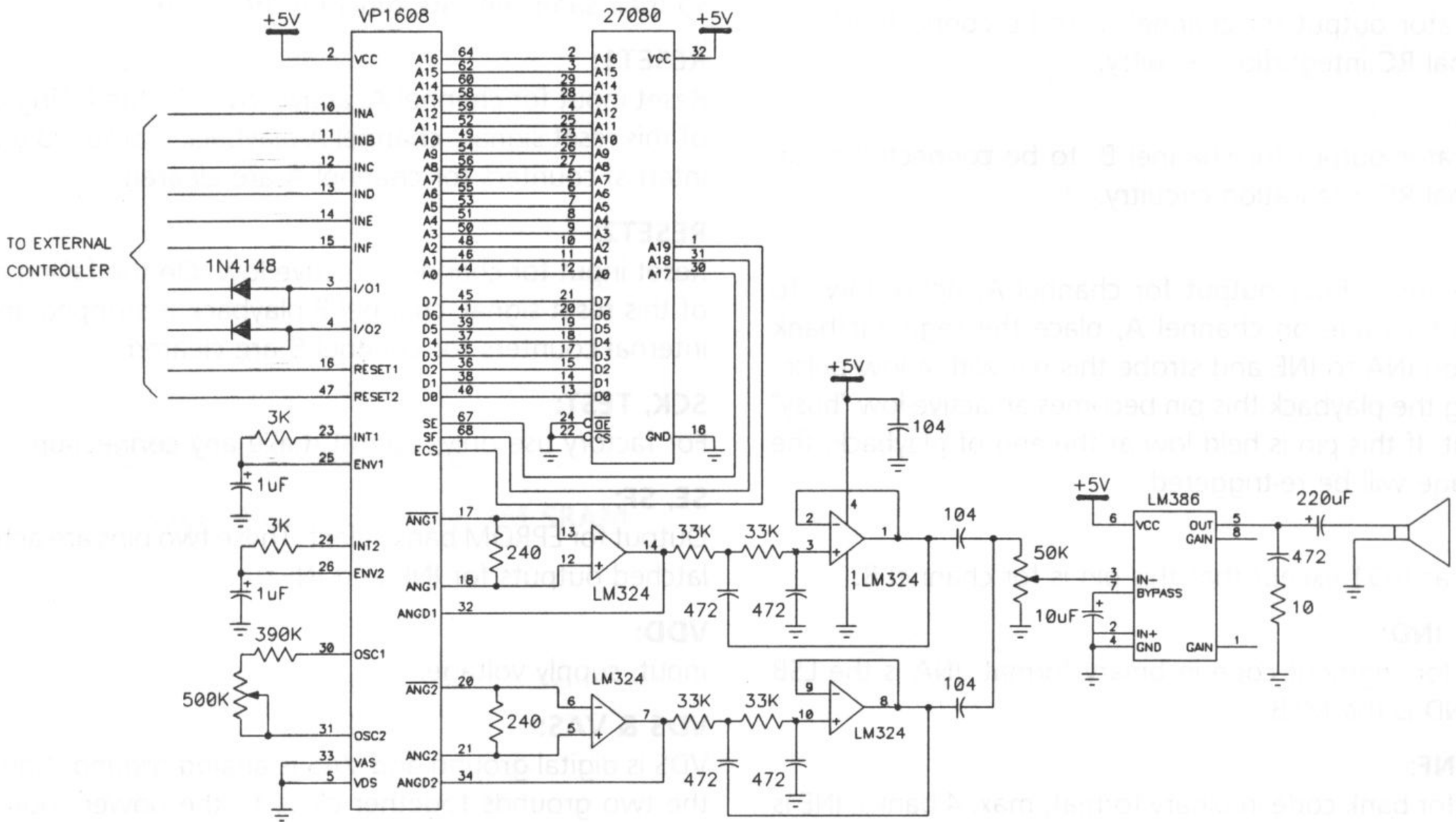
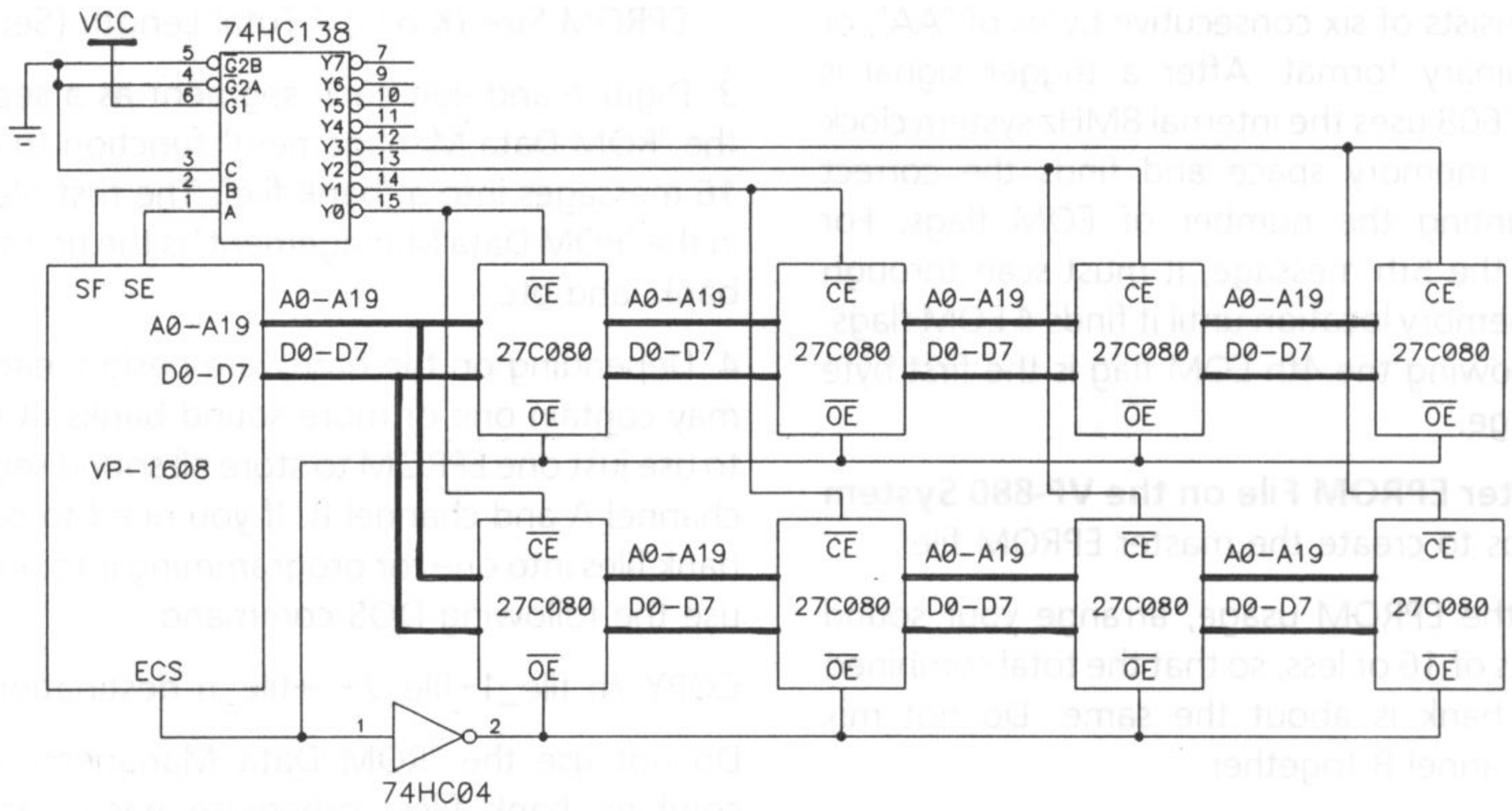
CIRCUIT DESIGN EXAMPLES

1. 64-Message/Channel Playback, 8M EPROM, Mixed Channel Output



2. Maximum EPROM Configuration For VP-1608



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